

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte RICHARD K. WILLIAMS  
and ROBERT G. BLATTNER

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Appeal No. 2000-0131  
Application No. 08/800,972

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ON BRIEF

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Before HAIRSTON, RUGGIERO, and GROSS, Administrative Patent Judges.  
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 16-20 and 24-32. Claims 1-15 and 23 have been canceled, and claims 21 and 22 have been allowed. Appellants' Brief (page 4) indicates that the appeal has been withdrawn with respect to claims

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16-20, 24-29, and 31 is before us on appeal. The appeal is dismissed as to claims 30 and 32.

The claimed invention relates to a bidirectional battery disconnect MOSFET switch which functions to block voltage in either direction when open and to conduct current in either direction when closed. The disconnect switch includes circuitry, referred to as a "body bias generator", which assures that the body of the MOSFET is shorted to whichever of the source/drain terminals of the MOSFET is biased at a lower voltage.

Claim 16 is illustrative of the invention and reads as follows:

16. An arrangement comprising:

a battery;

a first MOSFET having a drain terminal, a source terminal, a body and a first gate, said drain terminal being connected to a negative terminal of said battery, said first MOSFET further comprising a first intrinsic diode between said body and said source terminal and a second intrinsic diode between said body and said drain terminal;

a body bias generator connected to said drain terminal and said source terminal of said first MOSFET, said body bias generator biasing said body of said first MOSFET to the lower of a drain

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a third MOSFET connected between said body and said drain terminal, said third MOSFET having a third gate connected to said source terminal; and

a gate control circuit, said gate control circuit alternately biasing said first gate to a voltage at said body so as to turn said first MOSFET off or to a positive voltage so as to turn said first MOSFET on,

wherein said second MOSFET is adapted to turn on and conduct a first current between said body and said source terminal at a voltage drop across said second MOSFET which is less than a first voltage drop required to turn on said first intrinsic diode and said third MOSFET is adapted to turn on and conduct a second current between said body and said drain terminal at a voltage drop across said third MOSFET which is less than a second voltage drop required to turn on said second intrinsic diode.

The Examiner's Answer cites the following prior art references:

Fuller et al. (Fuller)	4,847,522	Jul. 11, 1989
Moyer et al. (Moyer)	5,430,403	Jul. 04, 1995
		(filed Sep. 20, 1993)

Claims 16-20, 24-29, and 31 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Fuller.<sup>2</sup>

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Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs<sup>3</sup> and Answer for the respective details.

#### OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner, the arguments in support of the rejection and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 16, 17, 19, and 25-29. We reach the opposite conclusion with respect to claims 18, 20, 24, and 31. Accordingly, we affirm-in-part.

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Appellants' arguments in response to the Examiner's obviousness rejection of the appealed claims are organized according to a suggested grouping of claims indicated at page 4 of the Brief. We will consider the appealed claims separately only to the extent separate arguments for patentability are presented. Any dependent claim not separately argued will stand or fall with its base claim. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745

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The Examiner's 35 U.S.C. § 103(a) rejection groups all of the appealed claims together and, as the basis for the obviousness rejection, the Examiner proposes to modify the output signal disable circuit disclosure of Fuller. According to the Examiner (Answer, page 7), Fuller discloses all of the claim limitations except for an explicit disclosure that the circuit power supply is a battery. The Examiner nevertheless asserts the manifest obviousness to the skilled artisan of using a battery as a circuit power supply.

With respect to independent claim 16 (the representative claim for Appellants' suggested grouping including claims 16, 17, and 19), after reviewing the Examiner's detailed analysis (Answer, pages 5-7), it is our view that such analysis carefully points out the teachings of the prior art Fuller reference, reasonably indicates the perceived differences between this prior art and the claimed invention, and provides reasons as to how and why the prior art teachings would have been modified to arrive at the claimed invention. In our opinion, the Examiner's analysis is sufficiently

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case of obviousness. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Brief have not been considered [see 37 CFR § 1.192(a)].

In response to the Examiner's obviousness rejection of representative independent claim 16, Appellants initially contend (Brief, page 6) that, contrary to the Examiner's position, Fuller does not provide for a "deadband" of voltages across the terminals of switch MOSFET 82 within which neither of the body bias generator transistors 84 and 86 is turned on. After careful review of the Fuller reference in light of the arguments of record, we are in agreement with the Examiner's position as expressed in the Answer.

As pointed out by the Examiner (Answer, page 9), the language of claim 16 does not require a "deadband" of voltages but, rather, only that the body of the switch MOSFET be biased to the lower of the drain voltage or source voltage "... when a difference between said drain and source voltages exceeds a predetermined level." We agree with the Examiner (id.) that the claimed "predetermined

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that would convince us of any error in the Examiner's line of reasoning (id. at 7) that the disclosed biasing function of the transistors 84 and 86 in Fuller would be defeated if the intrinsic diodes of the MOSFET switch 82 were allowed to turn on at a voltage drop less than that of the voltage drops across the transistors 84 and 86.

For the above reasons, it is our opinion that, since the Examiner's prima facie case of obviousness has not been rebutted by any convincing arguments from Appellants, the Examiner's obviousness rejection of representative independent claim 16, and claims 17 and 19 which fall with claim 16, is sustained.

We also sustain the Examiner's 35 U.S.C. § 103(a) rejection of independent claims 25 and 26 (the representative claim for Appellants' suggested grouping of claims 26-29) based on Fuller. In contrast to the "predetermined level" language of claim 16 discussed supra, independent claims 25 and 26 specifically require operation of the body bias generator transistors in relation to a predetermined voltage interval which defines a "deadband" range.



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which case neither of the body bias transistors 84 and 86 are turned on.

In reaching this conclusion, we are further persuaded by the Examiner's presentation of evidence in the form of the Moyer reference which, in analyzing the operation of the Fuller circuit, discloses that both of Fuller's body bias transistors are "... off simultaneously whenever the voltages at the drain and source of transistor **10** are very nearly the same." (Moyer, column 1, lines 59-63). As pointed out by the Examiner (Answer, page 6), although the language "very nearly the same" implies a very small voltage range, it nonetheless clearly indicates a non-zero interval or "deadband" during which both body bias transistors in Fuller are simultaneously off.

Turning to a consideration of the Examiner's 35 U.S.C. § 103(a) rejection of claims 18, 20, 24, and 31, we note that, while we found Appellants' arguments to be unpersuasive with respect to claims 16, 17, 19, and 25-29 discussed supra, we reach the opposite conclusion with respect to claims 18, 20, 24, and 31.

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terminal of switch MOSFET 82 as claimed. We agree with Appellants that, according to conventional usage, the Figure 4 illustration in Fuller, as well as the accompanying description beginning at column 8, line 43, indicates only that transistor 96 is connected to the source terminal, not the drain terminal, of switch MOSFET 82. Accordingly, because the Examiner has not established a prima facie case of obviousness since all of the claim limitations are not taught or suggested by the prior art, the obviousness rejection of claim 18 is not sustained.

Turning to a consideration of the Examiner's 35 U.S.C. § 103(a) rejection of independent claim 20, and its dependent claim 31, we do not sustain the rejection of these claims as well. Independent claim 20 concludes with a recitation of a specific range of peak parasitic current gain in the switch MOSFET of "greater than zero and less than or equal to 330." We find no basis in the disclosure of Fuller, nor is there any evidence forthcoming from the Examiner, that would support the Examiner's conclusion that such a range of parasitic current gain would be

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61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002). Our review of Fuller reveals no mention of parasitic current gain levels, let alone any structural arrangement that would reduce parasitic current gain to the specific level set forth in appealed claim 20.

Similarly, with respect to independent claim 24, which sets forth a specific threshold turn on voltage for the body bias transistors of "less than 640 mv", we find no evidence that would support the Examiner's assertion of obviousness. We do initially note, as discussed previously, that Appellants have not provided any persuasive evidence that would convince us that the Examiner has erred in concluding that the body bias transistors in Fuller, in order to perform their function, would necessarily turn on before the turn on of the intrinsic diodes of the MOSFET switch. We find, however, no evidence provided by the Examiner that would support the assertion that "... a standard diode is notoriously well known to have a 640 mv diode drop" (Answer, page 8) and, accordingly, we find the Examiner's conclusion that Fuller's body bias transistor turn on voltage would necessarily be less than 640

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reviewing court requires this evidence in order to establish a prima facie case. In re Knapp-Monarch Co., 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); In re Cofer, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966).

In summary, with respect to the Examiner's 35 U.S.C. § 103(a) rejection of the appealed claims, we have sustained the rejection of claims 16, 17, 19, and 25-29, but have not sustained the rejection of claims 18, 20, 24, and 31. Therefore, the Examiner's decision rejecting claims 16-20, 24-29, and 31 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
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	)	BOARD OF PATENT
JOSEPH F. RUGGIERO	)	APPEALS
Administrative Patent Judge	)	AND
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